

N-Channel MOSFET

Lead Free Package and Finish

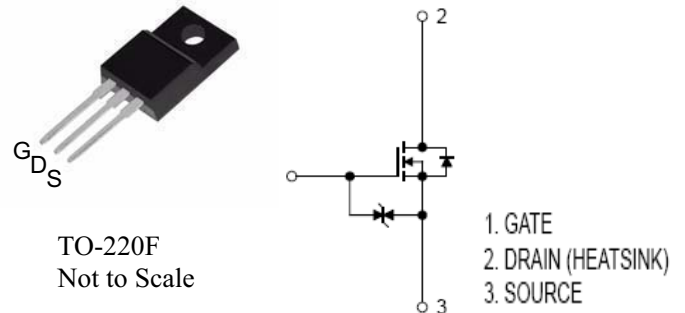
Applications:

- ATX Power
- LCD Panel Power

V _{DSS}	R _{DS(on)} (Typ)	I _D (Max)
900V	1.2Ω	9.0A

Features:

- RoHS Compliant & Halogen Free
- Low ON Resistance
- Low Gate Charge
- ESD Capability Improved



Ordering Information

Part Number	Package Type	Brand
ISA09N90A	TO-220F	IPS

Absolute Maximum Ratings T_c= 25°C unless otherwise specified

Symbol	Parameter	Maximum	Units
V _{DSS}	Drain-to-Source Voltage (NOTE *1)	900	V
I _D	Continuous Drain Current	9.0	A
I _{D@ 100 °C}	Continuous Drain Current	Figure3	
I _{DM}	Pulsed Drain Current, V _{GS@ 10V} (NOTE *2)	Figure6	
P _D	Power Dissipation	60	W
	Derating Factor above 25°C	0.48	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy(L=20mH);	500	mJ
V _{ESD(GS)}	Gate Source ESD Voltage(HBM,c=100pF,R=1.5K Ω)	6000	V
dv/dt	Peak Diode Recovery dv/dt (NOTE *3)	5.0	V/ns
T _L T _{PKG}	Maximum Temperature for Soldering Leads at 0.063in(1.6mm) from Case for 10 seconds Package Body for 10 seconds	300 260	°C
T _J and T _{STG}	Operation Junction and Storage Temperature Range	150, -55 to 150	°C

Caution: Stresses greater than those listed in "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	Maximum	Units	Test Condition
R _{θJC}	Junction-to-Case	2.08	°C/W	Drain lead soldered to water cooled heatsink, P _D ad-justed for a peak junction temperature of +150oC. 1 cubic foot chamber, free air.
R _{θJA}	Junction-to-Ambient	100		

Electrical Characteristics TJ= 25°C unless otherwise specified:

OFF Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
V _{DSS}	Drain-to-Source Breakdown Voltage	900	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	--	0.5	--	V/°C	Reference to 25°C, I _D =250uA
I _{DS(off)}	Off-State Drain-to-Source Current	--	--	1.0	uA	V _{DS} = 900V, V _{GS} =0V, T _a = 25°C
		--	--	250		V _{DS} = 720V, V _{GS} = 0 V, T _a = 125°C
I _{GSS(F)}	Gate-to-Source Forward Leakage	--	--	1.0	uA	V _{GS} =+20V
I _{GSS(R)}	Gate-to-Source Reverse Leakage	--	--	-1.0		V _{GS} =-20V

ON Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
R _{DS(ON)}	Drain-to-Source On-Resistance	--	1.20	1.4	Ω	V _{GS} =10V, I _D =4.5A (NOTE*4)
g _{fs}	Forward Transconductance	--	10	--	S	V _{DS} >2I _D *R _{DS(on)} _{max} I _D =9A (NOTE*4)
V _{GS(TH)}	Gate Threshold Voltage	2.0	--	4.0	V	V _{DS} = V _{GS} , I _D = 250μA

Dynamic Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
C _{iss}	Input Capacitance	--	2100	--	pF	V _{GS} =0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	--	152	--		
C _{rss}	Reverse Transfer Capacitance	--	12	--		
Q _g	Total Gate Charge	--	47	--	nC	V _{DD} =450V I _D =9.0A V _{gs} =10V
Q _{gs}	Gate-to-Source Charge	--	10	--		
Q _{gd}	Gate-to-Drain ("Miller")Charge	--	17	--		

Resistive Switching Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
t _{d(ON)}	Turn-on Delay Time	--	16	--	ns	V _{DD} = 450V I _D =4.0A V _{GS} = 10V R _G =4.7Ω
trise	Rise Time	--	10	--		
t _{d(OFF)}	Turn-Off Delay Time	--	50	--		
t _{fall}	Fall Time	--	23	--		

Source-Drain Diode Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
I_S	Continuous Source Current (Body Diode)	--	--	9.0	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	36	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_S=9.0A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	305	--	nS	$I_F=9.0A,$ $T_j = 25^\circ C$ $di/dt=100A/us$
Q_{rr}	Reverse Recovery Charge	--	2.2	--	μC	

Notes:

-
- *1. $T_j=+25^\circ C$ to $+150^\circ C$.
 - *2. Repetitive rating; pulse width limited by maximum junction temperature.
 - *3. $I_{SD}=9.0A$ $di/dt \leq 100A/us$, $V_{DD} \leq BV_{DSS}$, $T_{jmax}=+150^\circ C$.
 - *4. Pulse width $\leq 380us$; duty cycle $\leq 2\%$.

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

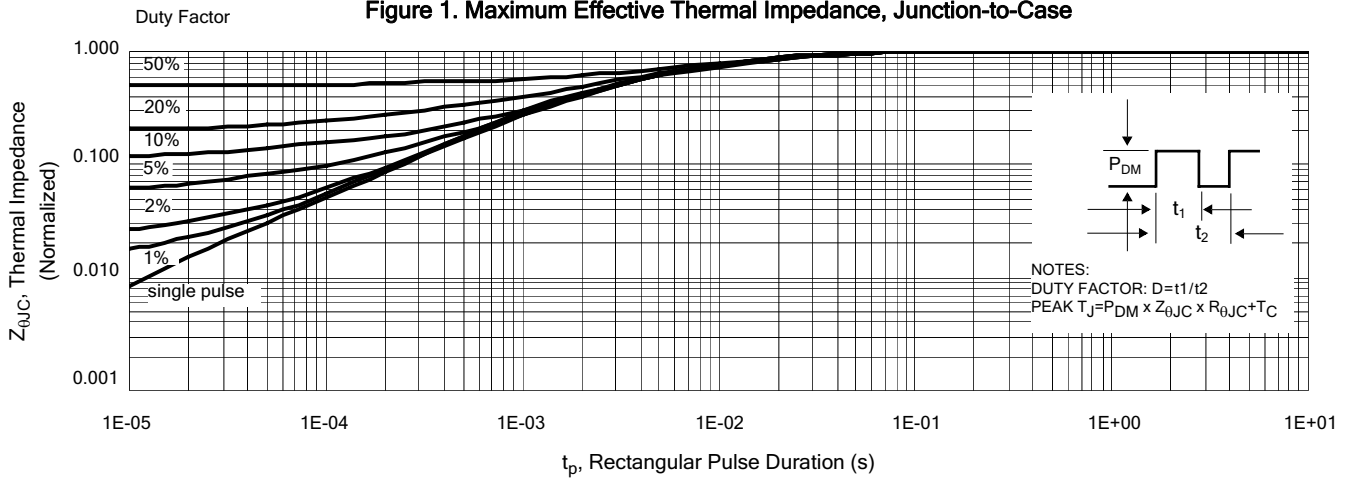


Figure 2. Maximum Power Dissipation vs Case Temperature

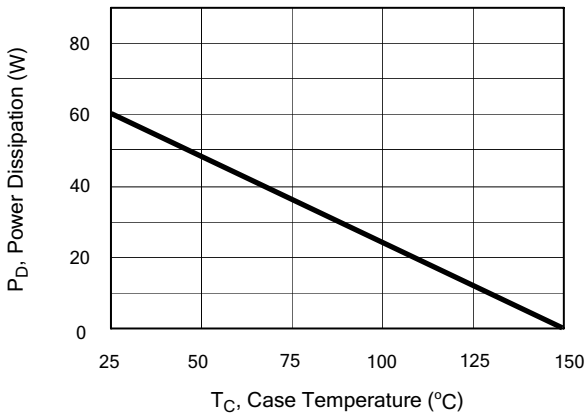


Figure 3. Maximum Continuous Drain Current vs Case Temperature

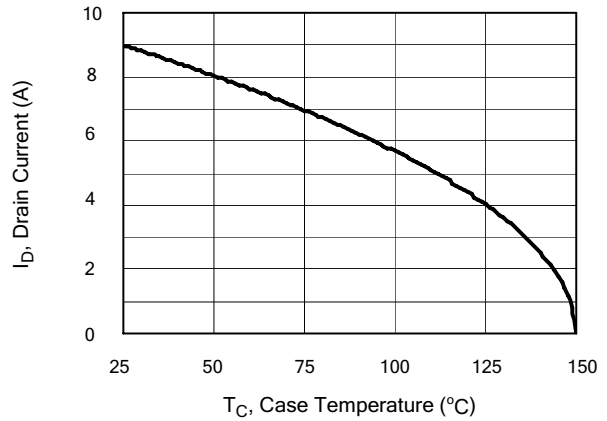


Figure 4. Typical Output Characteristics

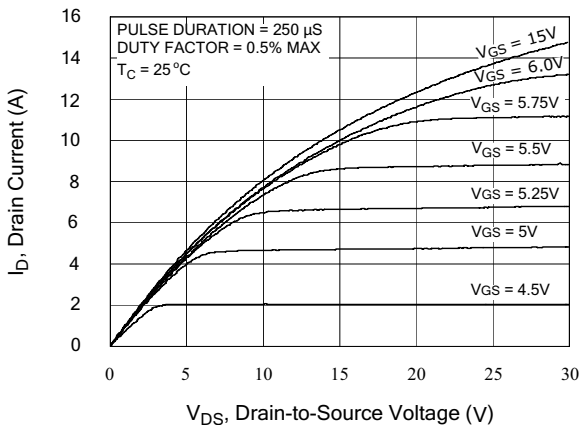


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

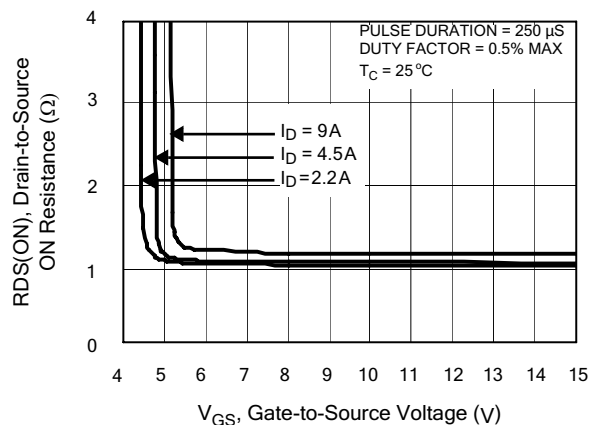


Figure 6. Maximum Peak Current Capability

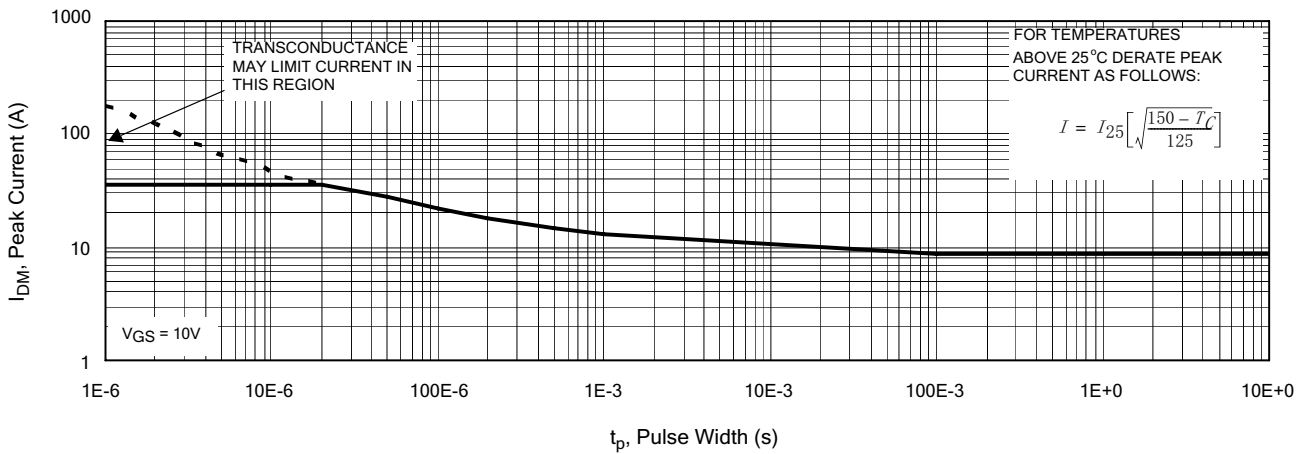


Figure 7. Typical Transfer Characteristics

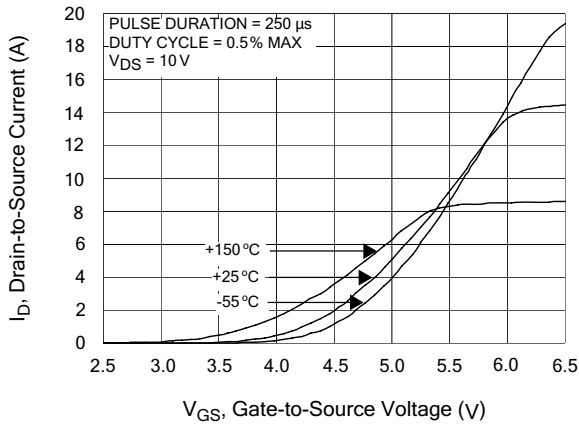


Figure 8. Unclamped Inductive Switching Capability

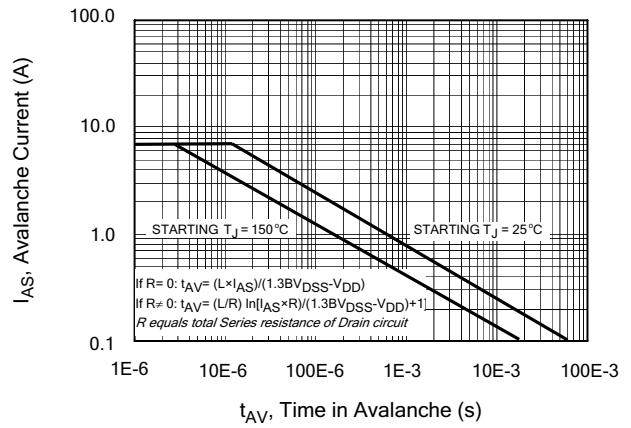


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

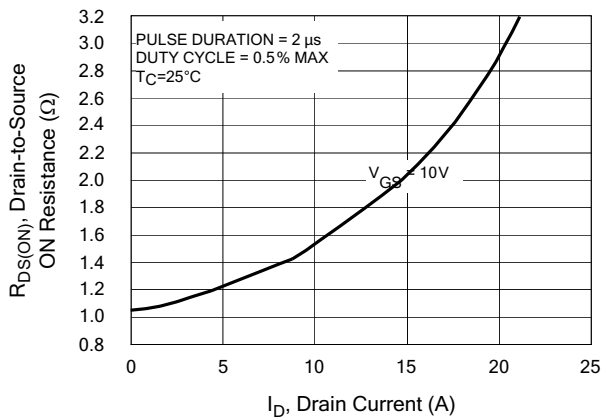


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

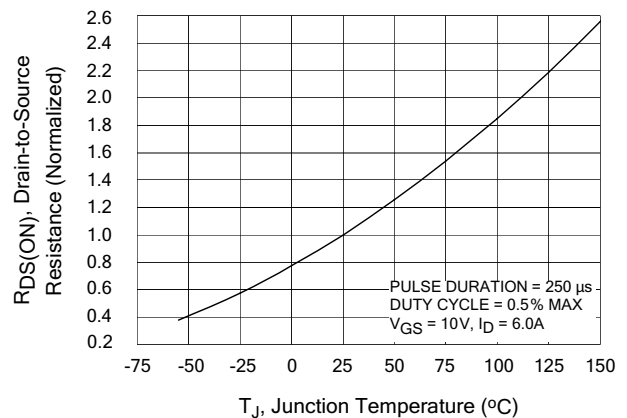


Figure 11. Typical Breakdown Voltage vs Junction Temperature

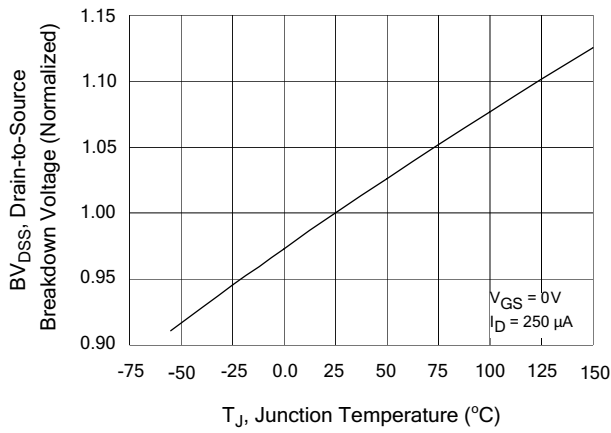


Figure 12. Typical Threshold Voltage vs Junction Temperature

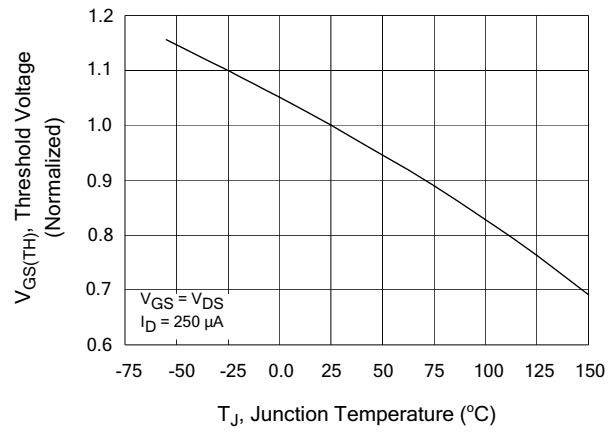


Figure 13. Maximum Forward Bias Safe Operating Area

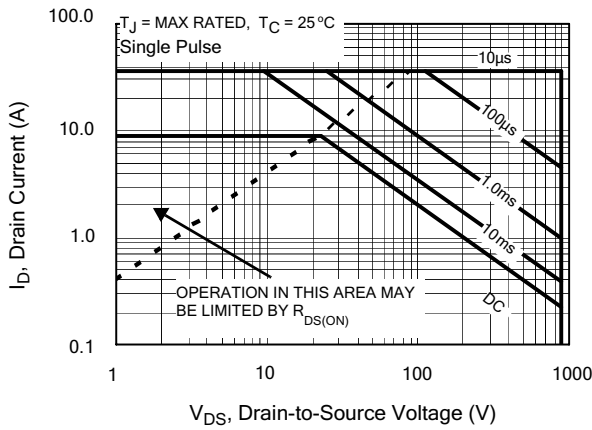


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

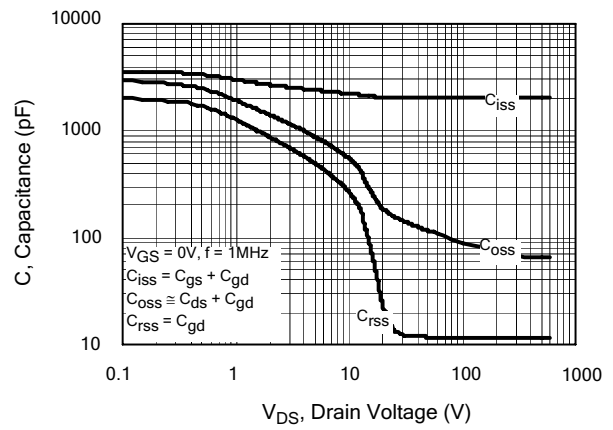


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

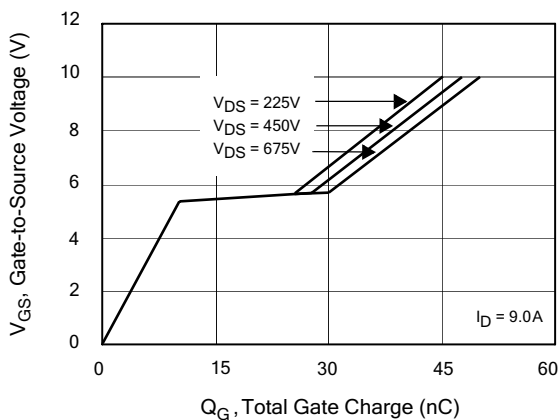
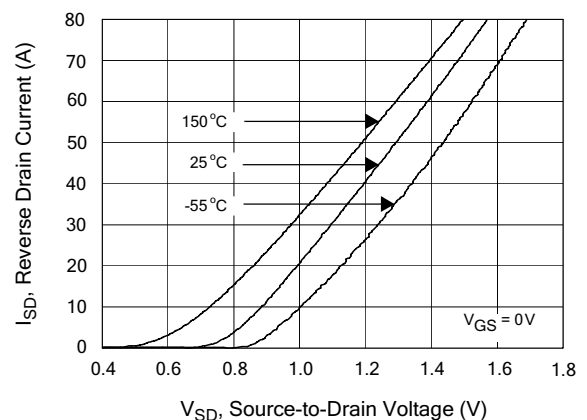


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

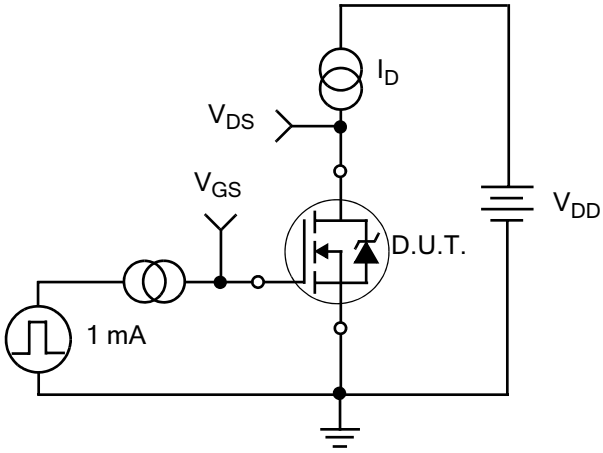


Figure 17. Gate Charge Test Circuit

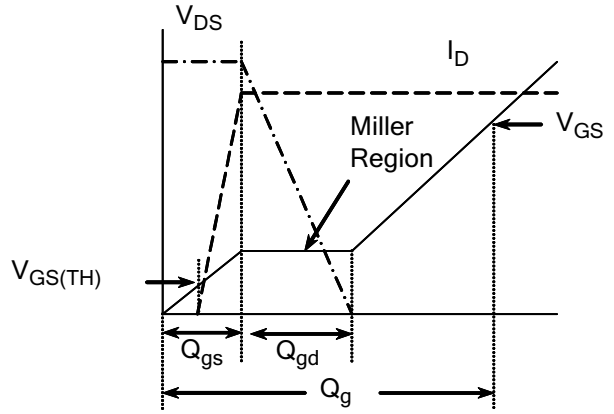


Figure 18. Gate Charge Waveform

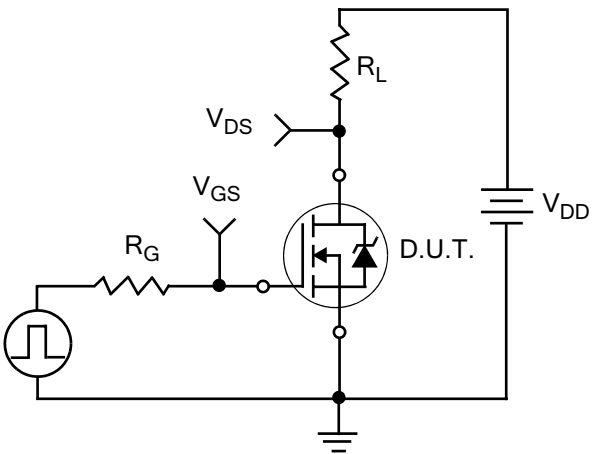


Figure 19. Resistive Switching Test Circuit

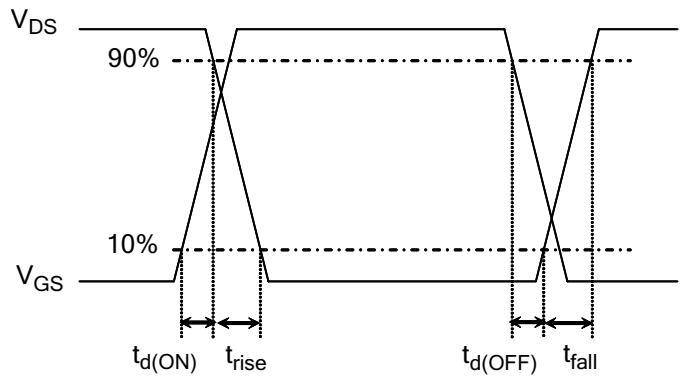


Figure 20. Resistive Switching Waveforms

Test Circuits and Waveforms

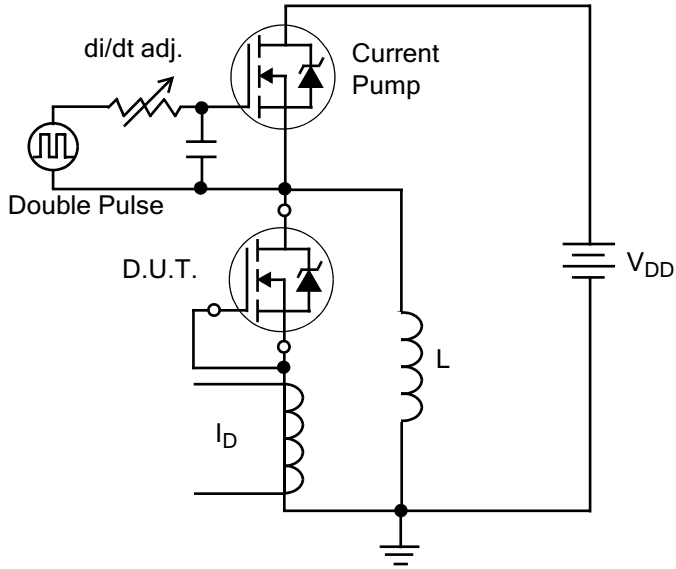


Figure 21. Diode Reverse Recovery Test Circuit

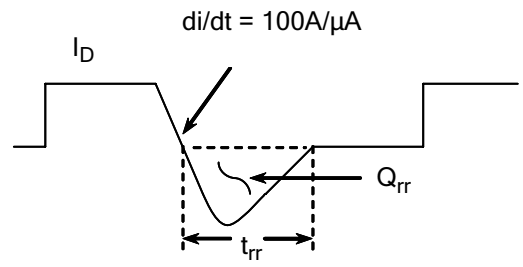


Figure 22. Diode Reverse Recovery Waveform

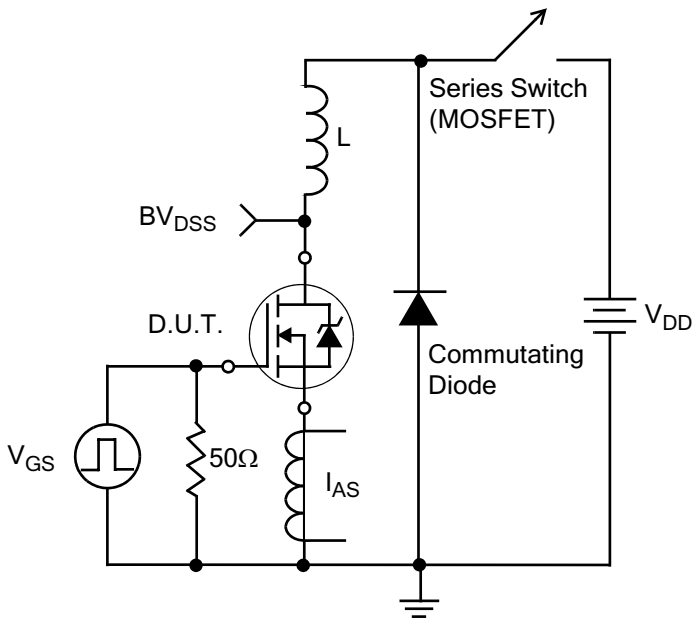


Figure 23. Unclamped Inductive Switching Test Circuit

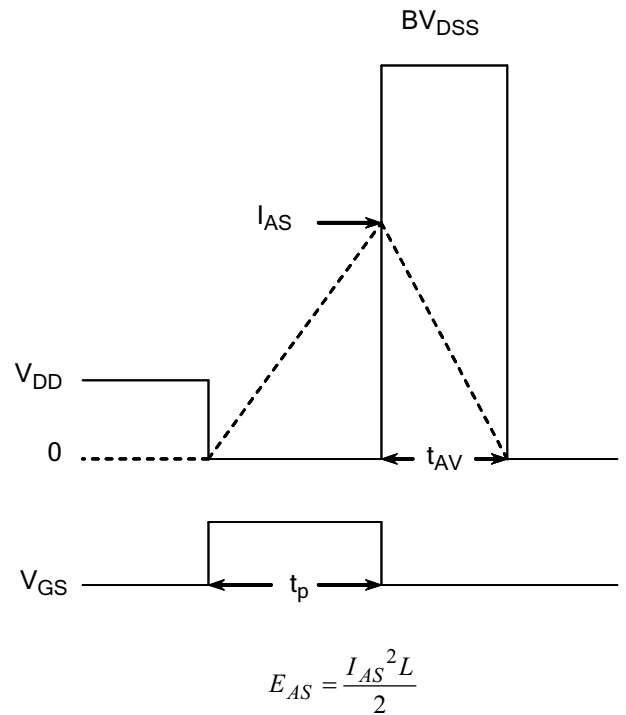


Figure 24. Unclamped Inductive Switching Waveforms

Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warranties for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

The MOSFET device is electrostatic sensitive. Proper electrostatic discharge (ESD) protection shall be implemented to avoid damaging the device.

Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
 - a. are intended for surgical implant into the human body,
 - b. support or sustain life,
 - c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.