

N-Channel MOSFET

Lead Free Package and Finish

Applications:

- Adaptor
- Charger
- SMPS

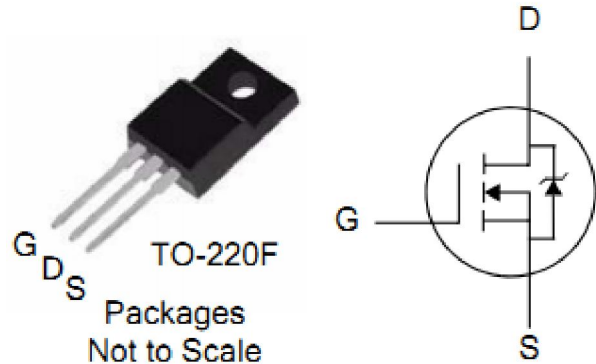
V_{DSS}	$R_{DS(ON)}(Typ.)$	I_D
600V	0.41Ω	16A

Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
ITA16N60A	TO-220F	IPS



Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	ITA16N60A	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	16	A
	Continuous Drain Current $T_C = 100^{\circ}C$	11.5	A
I_{DM}	Pulsed Drain Current, $V_{GS}@10V$ (NOTE *1)	64	A
P_D	Power Dissipation	70	W
	Derating Factor above $25^{\circ}C$	0.56	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	1000	mJ
dv/dt	Peak Diode Recovery dv/dt(NOTE *3)	5	V/ns
T_L	Maximum Temperature for Soldering	300	$^{\circ}C$
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150, -55 to 150	

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.79	$^{\circ}C/W$	Water cooled heatsink, P_D adjusted for a peak junction temperature of $+150^{\circ}C$.
$R_{\theta JA}$	Junction-to-Ambient	100		1 cubic foot chamber, free air.



ITA16N60A

OFF Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=600V, V_{GS}=0V$ $T_J=25^\circ\text{C}$
		--	--	100		$V_{DS}=480V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	$V_{GS}=+30V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-30V$

ON Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.41	0.5	Ω	$V_{GS}=10V, I_D=8A$
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
g_{fs}	Forward Transconductance	--	15	--	S	$V_{DS}=15V, I_D=8A$

Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2442	--	μF	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$
C_{oss}	Output Capacitance	--	218	--		
C_{rSS}	Reverse Transfer Capacitance	--	18.5	--		
Q_g	Total Gate Charge	--	54	--	nC	$I_D=16A, V_{DD}=300V$ $V_{GS}=10V$
Q_{gs}	Gate-to-Source Charge	--	12	--		
Q_{gd}	Gate-to-Drain ("Miller") Charge	--	21	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	ns	$V_{DD}=300V, I_D=16A,$ $V_G=10V R_G=6.1\Omega$
t_{rise}	Rise Time	--	52	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	59	--		
t_{fall}	Fall Time	--	72	--		



Source-Drain Diode Characteristics $T_c=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	16	A	$T_c=25^\circ\text{C}$
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	64	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_{SD}=16\text{A}, V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	--	380	--	ns	$I_F=I_S$ $di/dt=100\text{A/us}$
Q_{rr}	Reverse Recovery Charge	--	2.6	--	μC	
Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$						

Notes:

- *1. Repetitive rating; pulse width limited by maximum junction temperature.
- *2. $L=10\text{mH}$, $I_D=14.2\text{A}$, Start $T_J=25^\circ\text{C}$
- *3. $I_{SD}=16\text{A}$, $di/dt \leq 100\text{A/us}$, $V_{DD} \leq BV_{DS}$, Start $T_J=25^\circ\text{C}$

Characteristics Curve:

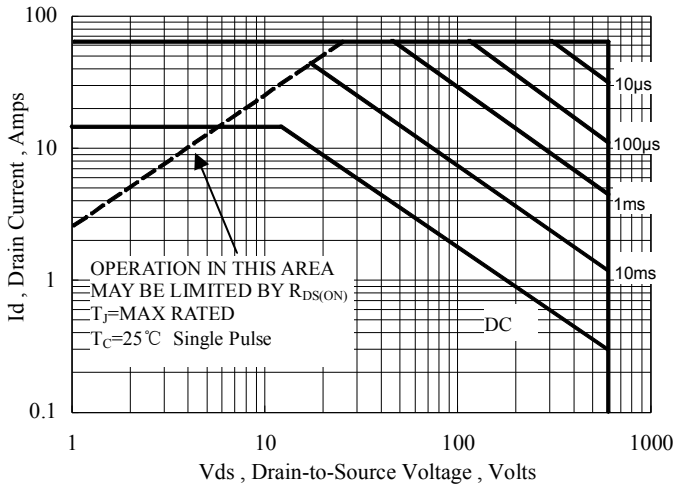


Figure 1 Maximum Forward Bias Safe Operating Area

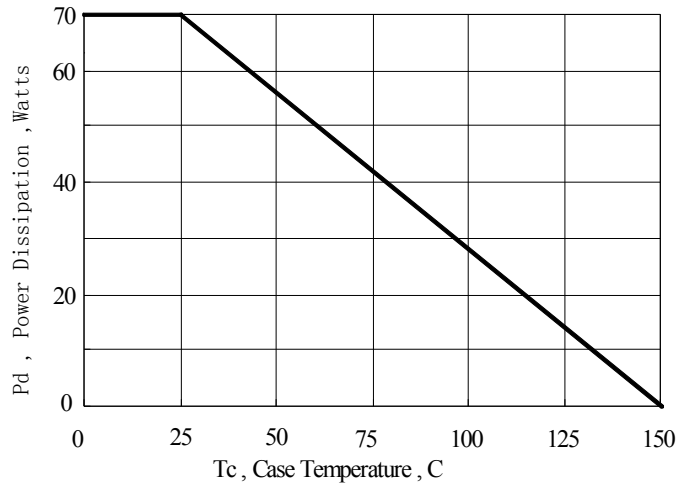


Figure 2 Maximum Power Dissipation vs Case Temperature

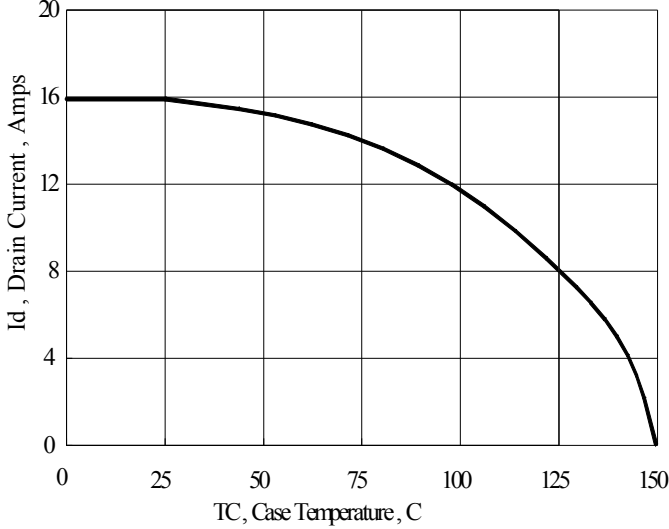


Figure 3 Maximum Continuous Drain Current vs Case Temperature

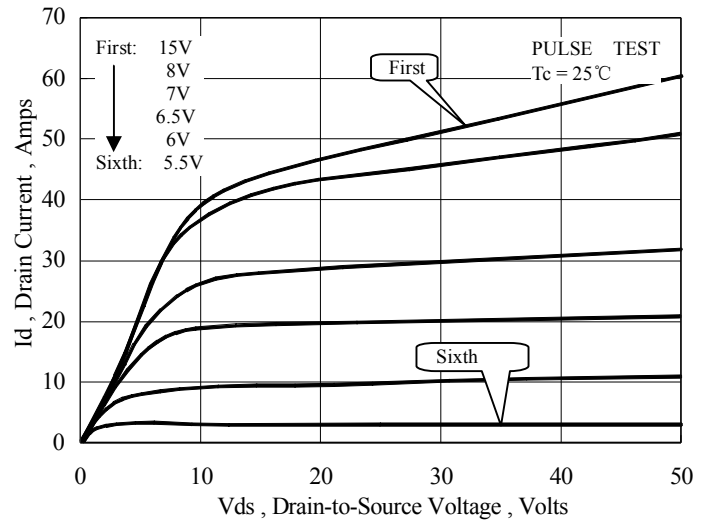


Figure 4 Typical Output Characteristics

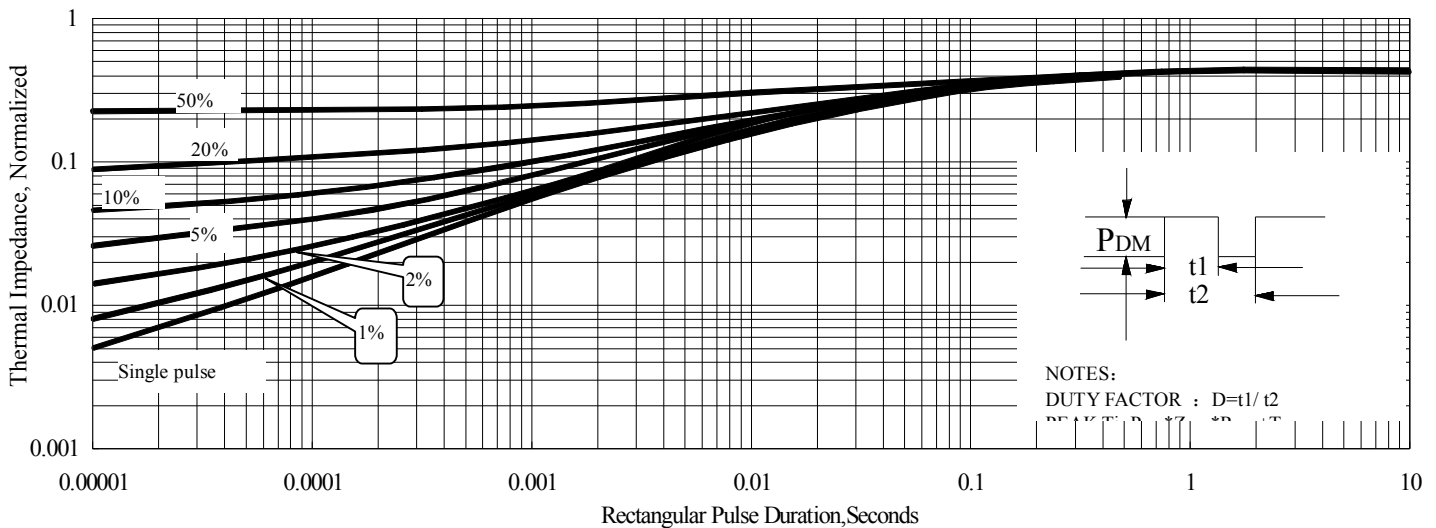


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

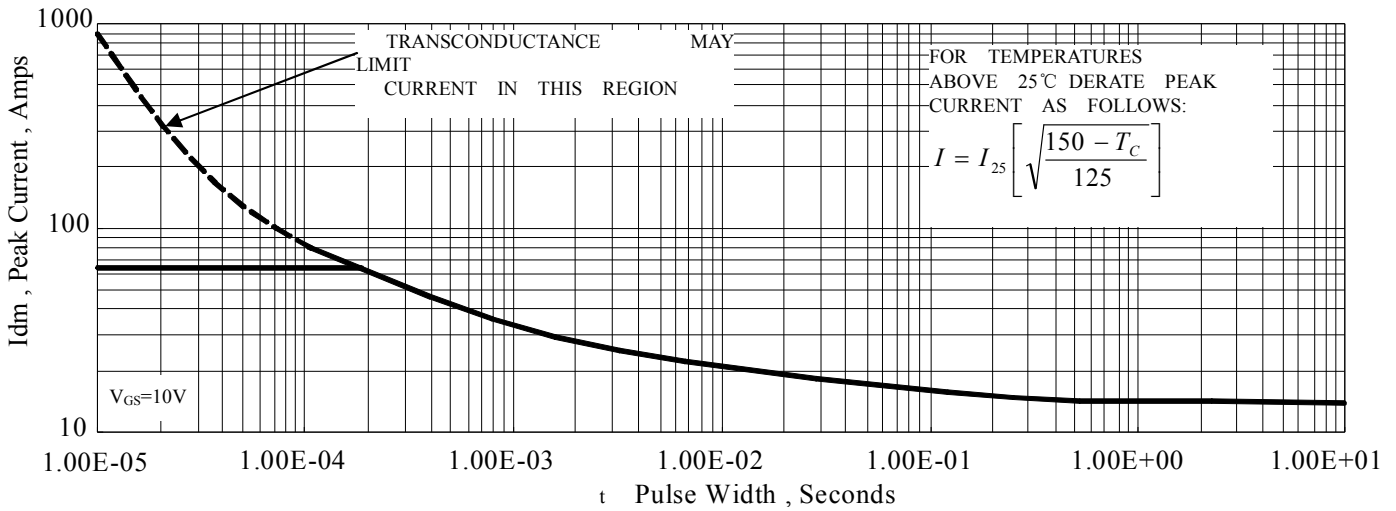


Figure 6 Maximum Peak Current Capability

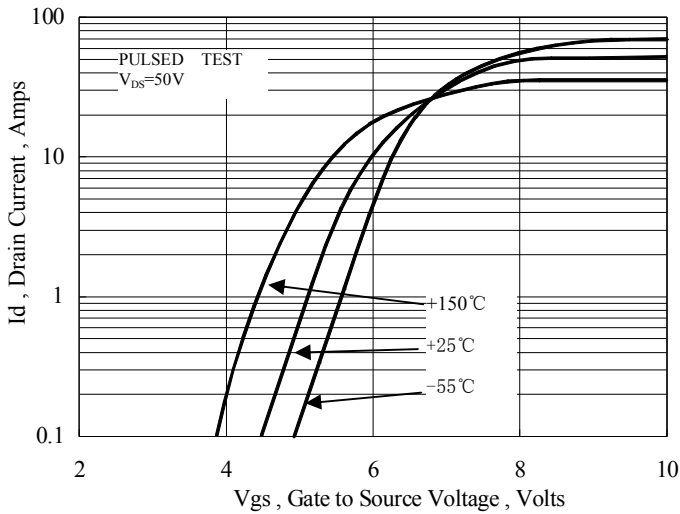


Figure 7 Typical Transfer Characteristics

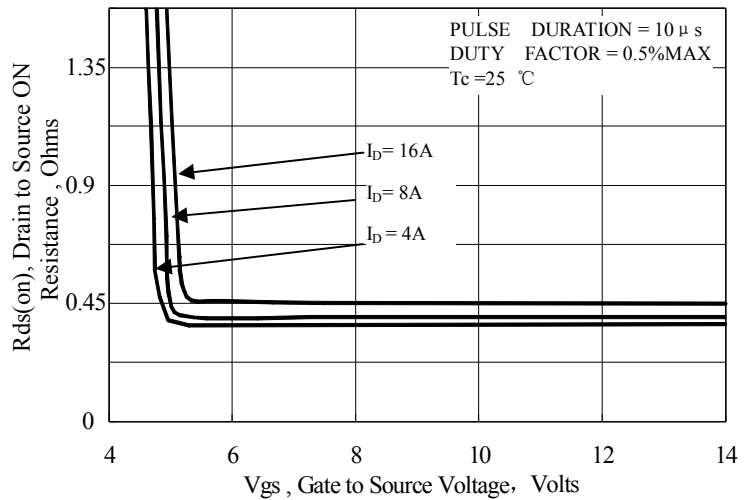


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

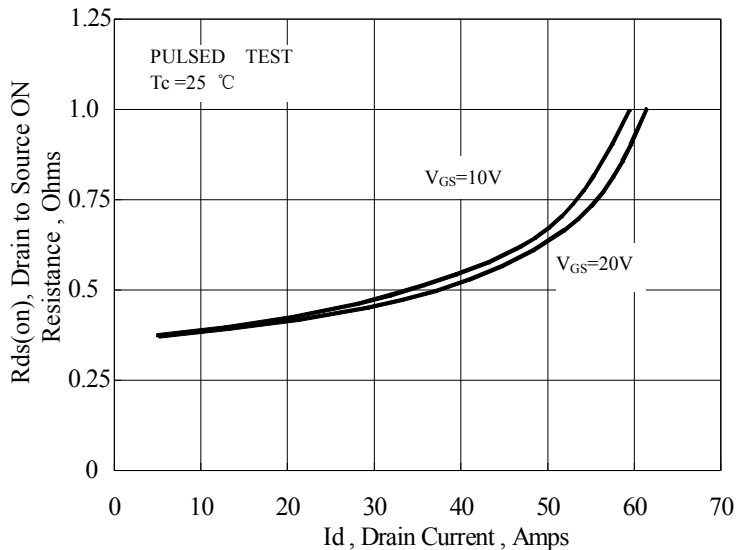


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

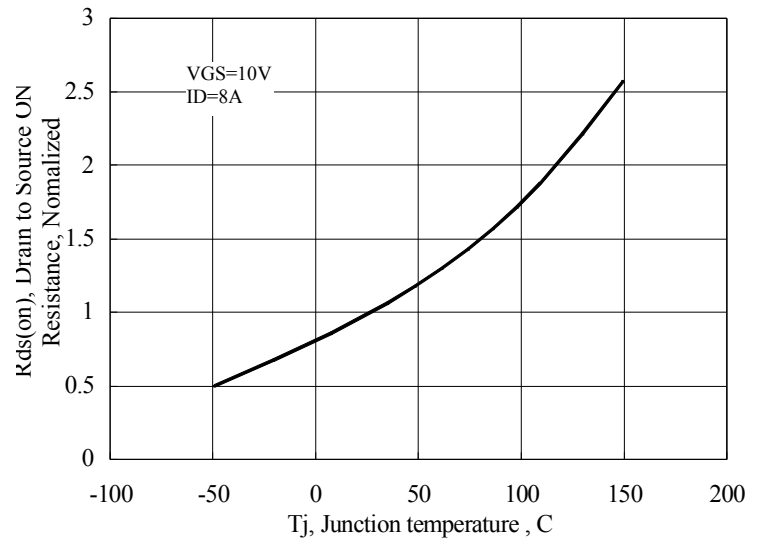


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature

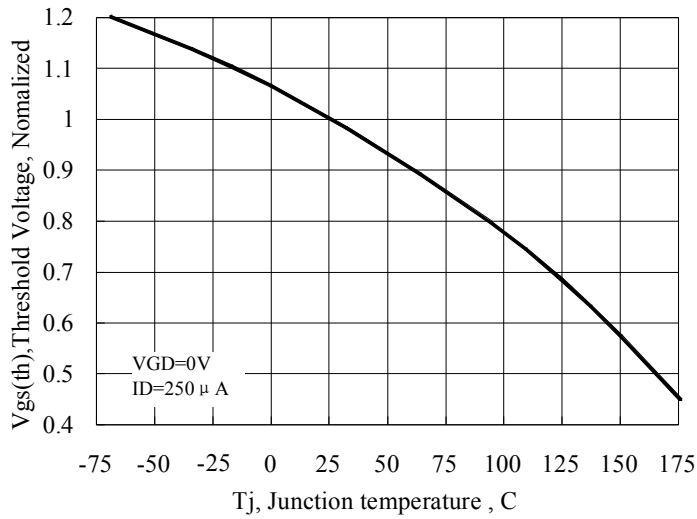


Figure 11 Typical Theshold Voltage vs Junction Temperature

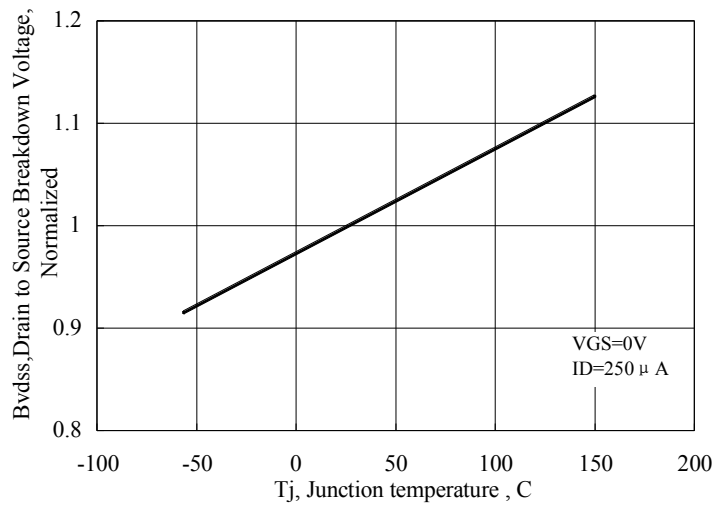


Figure 12 Typical Breakdown Voltage vs Junction Temperature

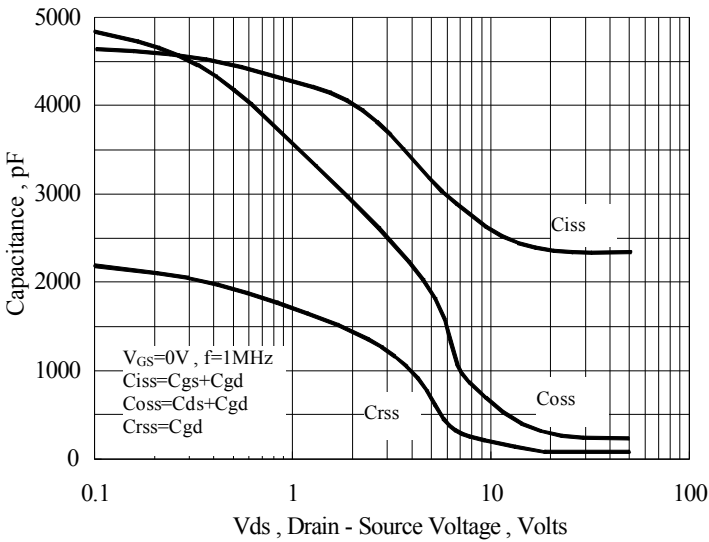


Figure 13 Typical Capacitance vs Drain to Source Voltage

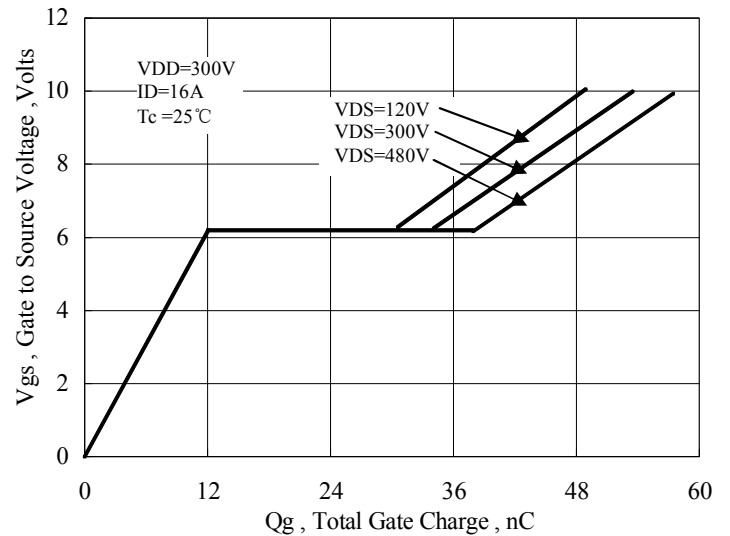


Figure 14 Typical Gate Charge vs Gate to Source Voltage

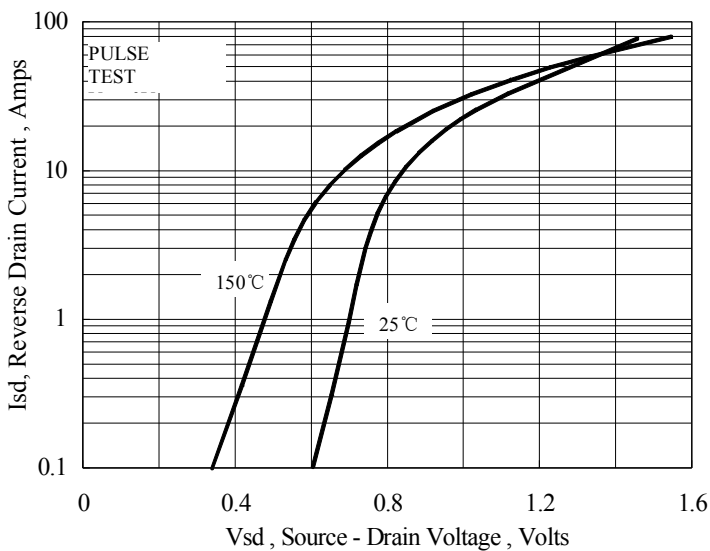


Figure 15 Typical Body Diode Transfer Characteristics

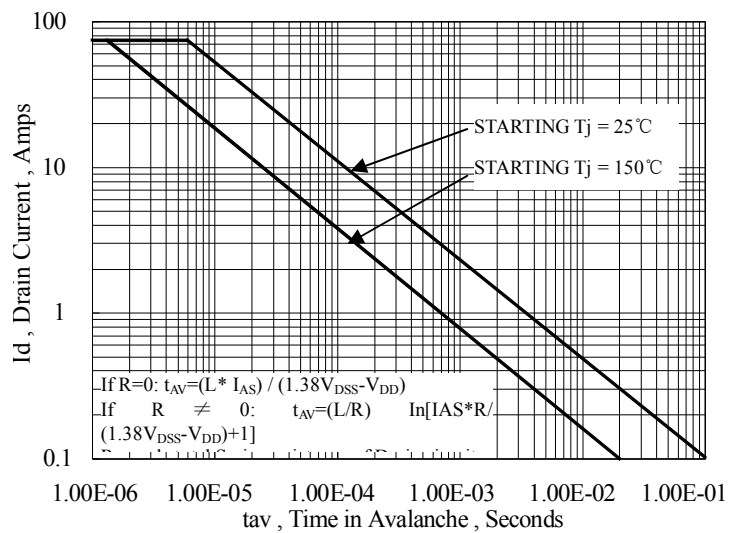


Figure 16 Unclamped Inductive Switching Capability

Test Circuits and Waveforms

Figure 17. Gate Charge Test Circuit

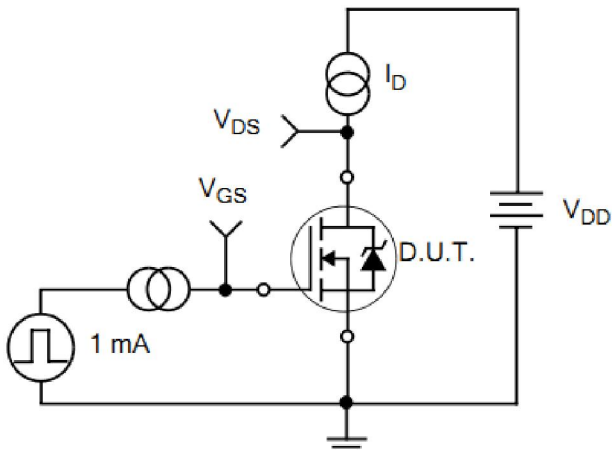


Figure 18. Gate Charge Waveforms

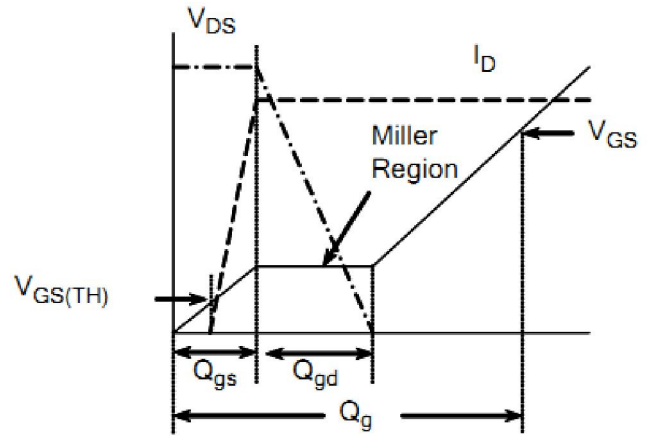


Figure 19. Resistive Switching Test Circuit

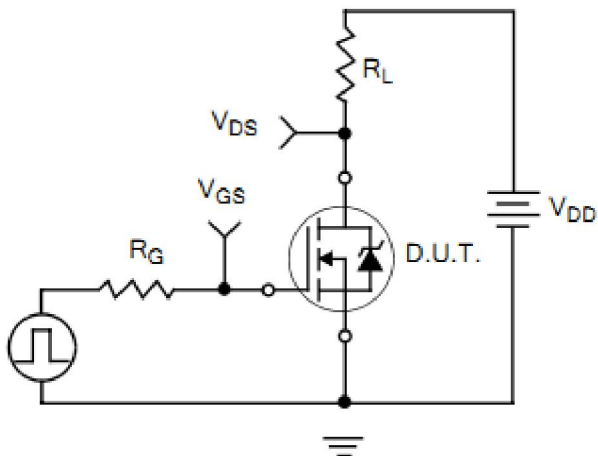


Figure 20. Resistive Switching Waveforms

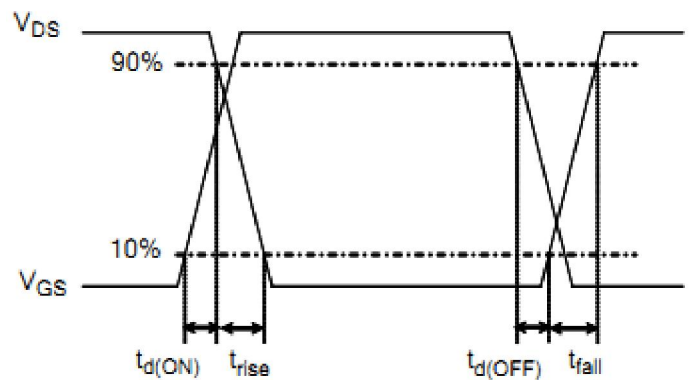


Figure 21. Diode Reverse Recovery Test Circuit

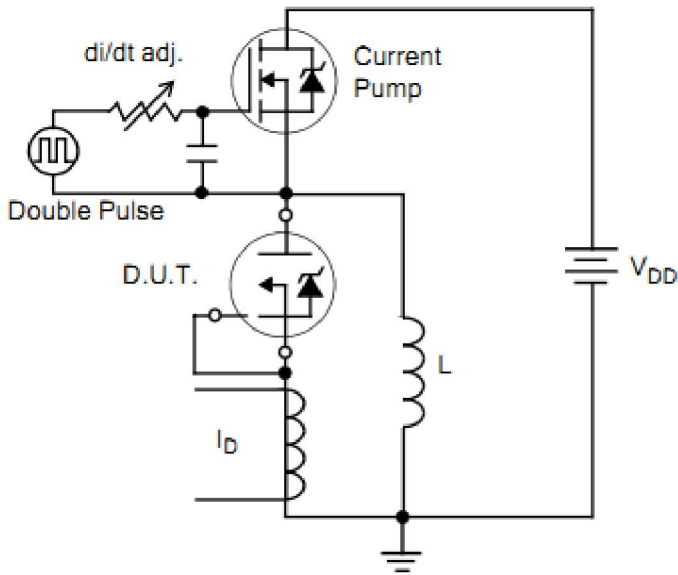


Figure 22. Diode Reverse Recovery Waveform

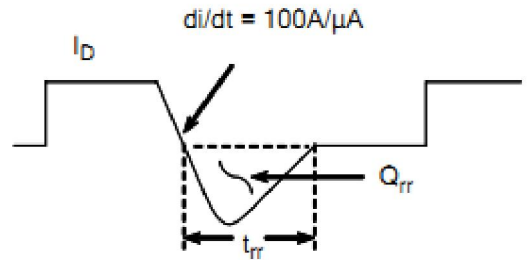


Figure 23. Unclamped Inductive Switching Test Circuit

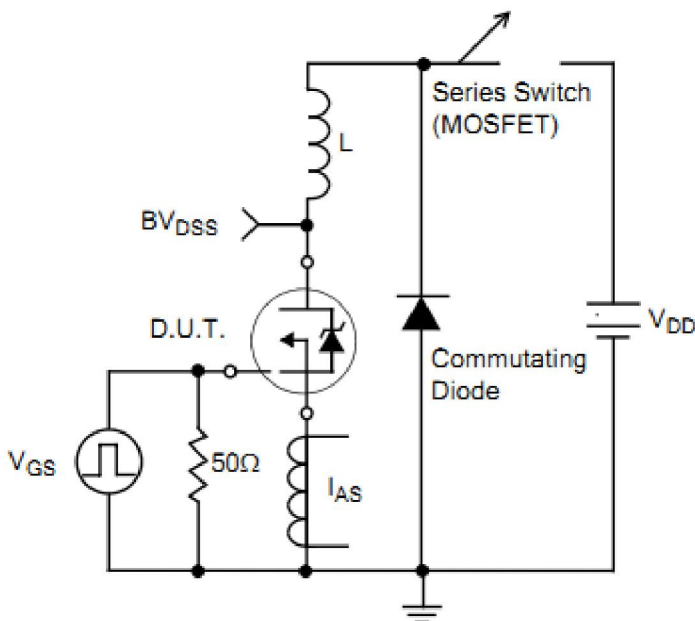
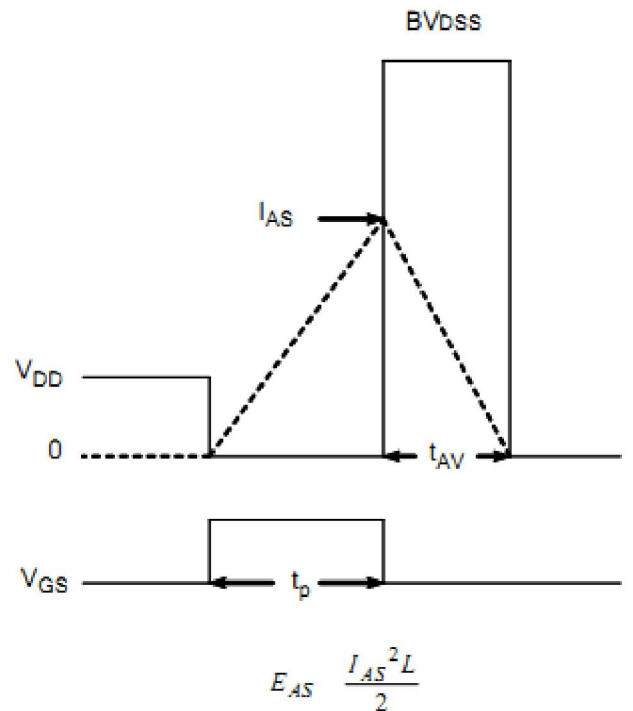


Figure 24. Unclamped Inductive Switching Waveform





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